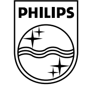
DATA SHEET

TDA1543
Dual 16-bit DAC (economy version) (I^2S input format)

Product specification
File under Integrated Circuits, IC01

February 1991

Philips
Semiconductors





FEATURES

- Low distortion
- 16-bit dynamic range
- 4 × oversampling possible
- Single 5 V power supply
- No external components required
- No requirement for external deglitcher circuitry due to fast settling output current
- Adjustable bias current
- Internal timing and control circuits
- I^2S input format: time multiplexed, two's complement, TTL.

GENERAL DESCRIPTION

The TDA1543 is a monolithic integrated dual 16-bit digital-to-analog converter (DAC) designed as an economy version for use in hi-fi digital audio equipment such as Compact Disc players, digital tape or cassette recorders, digital sound in TV sets and in digital amplifiers.

ORDERING INFORMATION

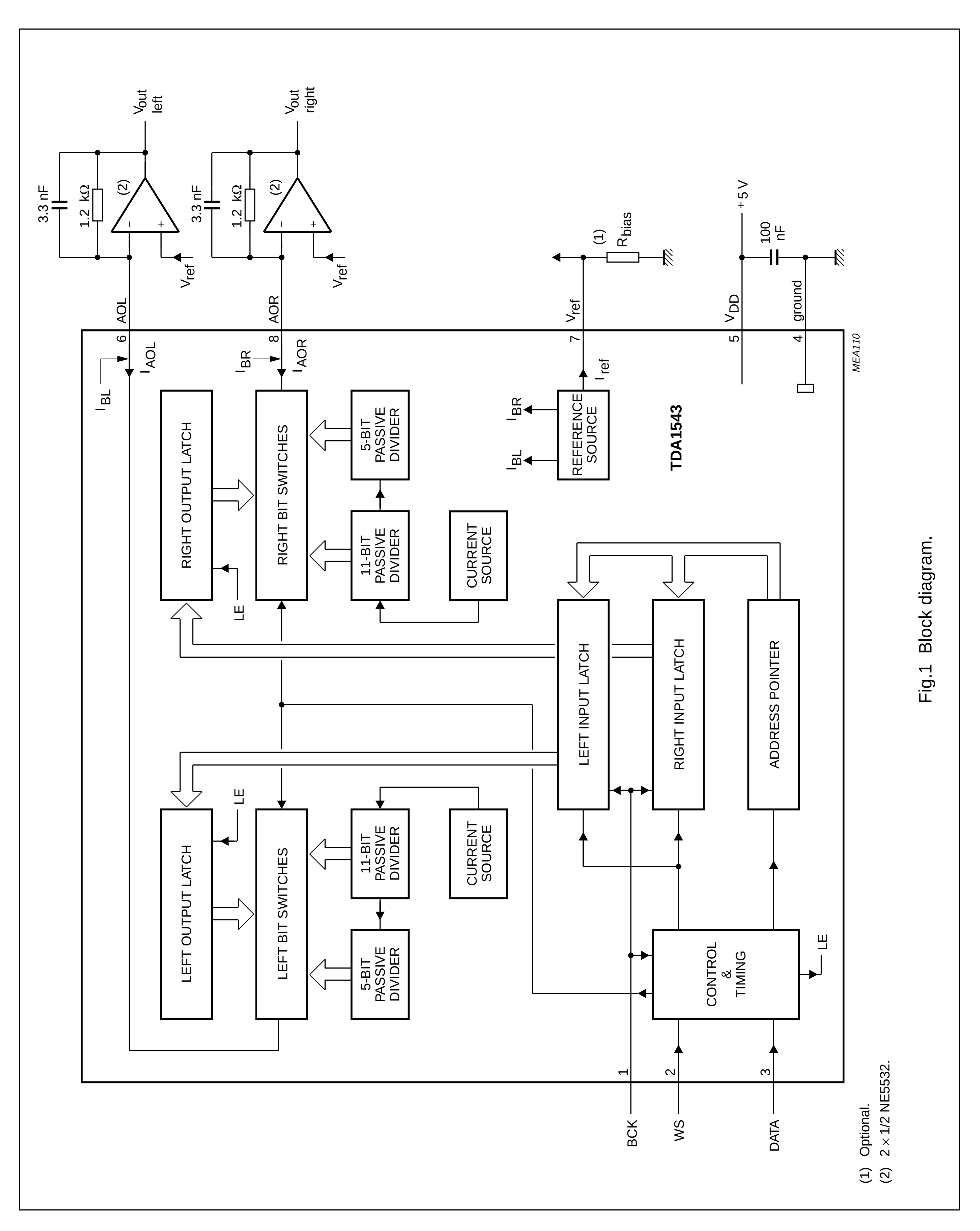
EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA1543(1)	8	DIL	plastic	SOT97
TDA1543T(2)	16	mini-pack	plastic	SO16L;SOT162A

Notes

1. SOT97-1; 1996 August 13.
2. SOT162-1 1996 August 13.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage		3.0	5.0	8.0	V
I_{DD}	supply current		–	50	60	mA
I_{FS}	full scale output current		1.95	2.30	2.65	mA
THD	total harmonic distortion	including noise	–	–75	–70	dB
		at 0 dB	–	0.018	0.032	%
THD	total harmonic distortion	including noise	–	–30	–23	dB
		at –60 dB	–	3.2	7.9	%
t_{cs}	current settling time to ± 1 LSB		–	0.5	–	µs
BR	input bit rate at data input		–	–	9.2	Mbits/s
f_{BCK}	clock frequency at clock input		–	–	9.2	MHz
S/N	signal-to-noise ratio	at bipolar zero	90	96	–	dB
TC_{FS}	full scale temperature coefficient	at analog outputs (AOL; AOR)	–	$\pm 500 \times 10^{-6}$	–	K^{-1}
T_{amb}	operating ambient temperature range		–30	–	+85	°C
P_{tot}	total power dissipation		–	250	–	mW
I_{bias}	bias current (adjustable)		–0.6	–	5.0	mA



(1) Optional.
(2) 2 × 1/2 NE5532.

Fig.1 Block diagram.

Dual 16-bit DAC (economy version) (I^2S input format)

TDA1543

PINNING

SYMBOL	PIN	DESCRIPTION
BCK	1	bit clock input
WS	2	word select input
DATA	3	data input
GND	4	ground
V_{DD}	5	+5 V supply voltage
AOL	6	left channel voltage output
V_{ref}	7	reference voltage output
AOR	8	right channel output

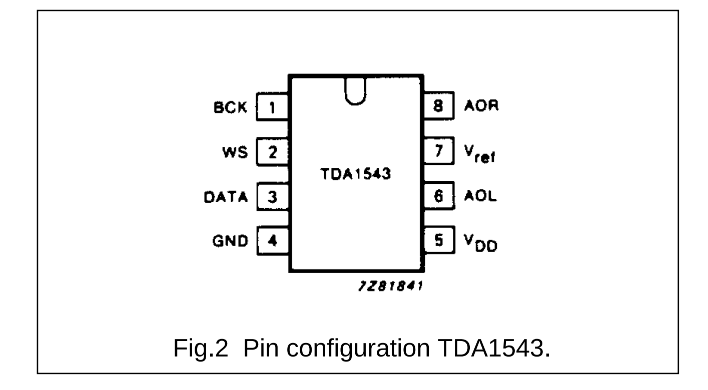


Fig.2 Pin configuration TDA1543.

PINNING

SYMBOL	PIN	DESCRIPTION
n.c.	1	not connected
n.c.	2	not connected
BCK	3	bit clock input
WS	4	word select input
DATA	5	data input
GND	6	ground
n.c.	7	not connected
n.c.	8	not connected
n.c.	9	not connected
n.c.	10	not connected
V_{DD}	11	+5 V supply voltage
AOL	12	left channel output
V_{ref}	13	reference voltage output
AOR	14	right channel output
n.c.	15	not connected
n.c.	16	not connected

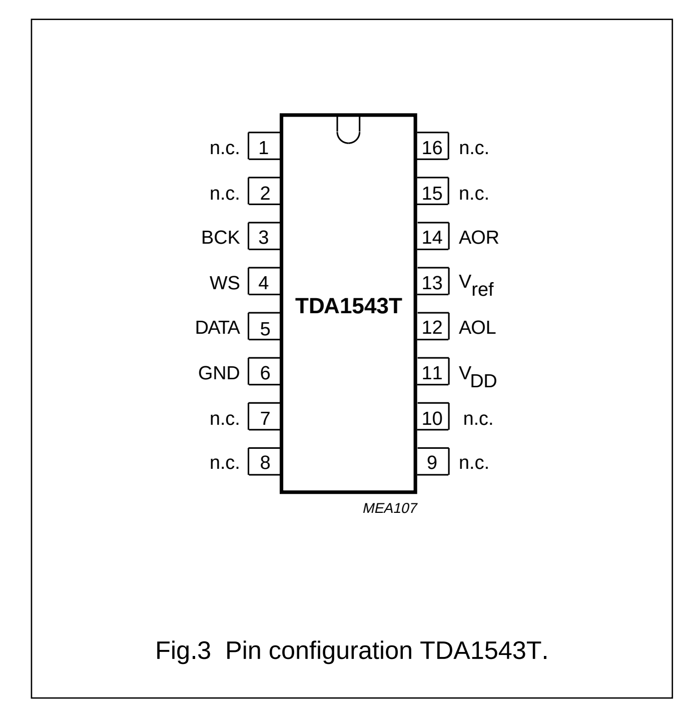


Fig.3 Pin configuration TDA1543T.

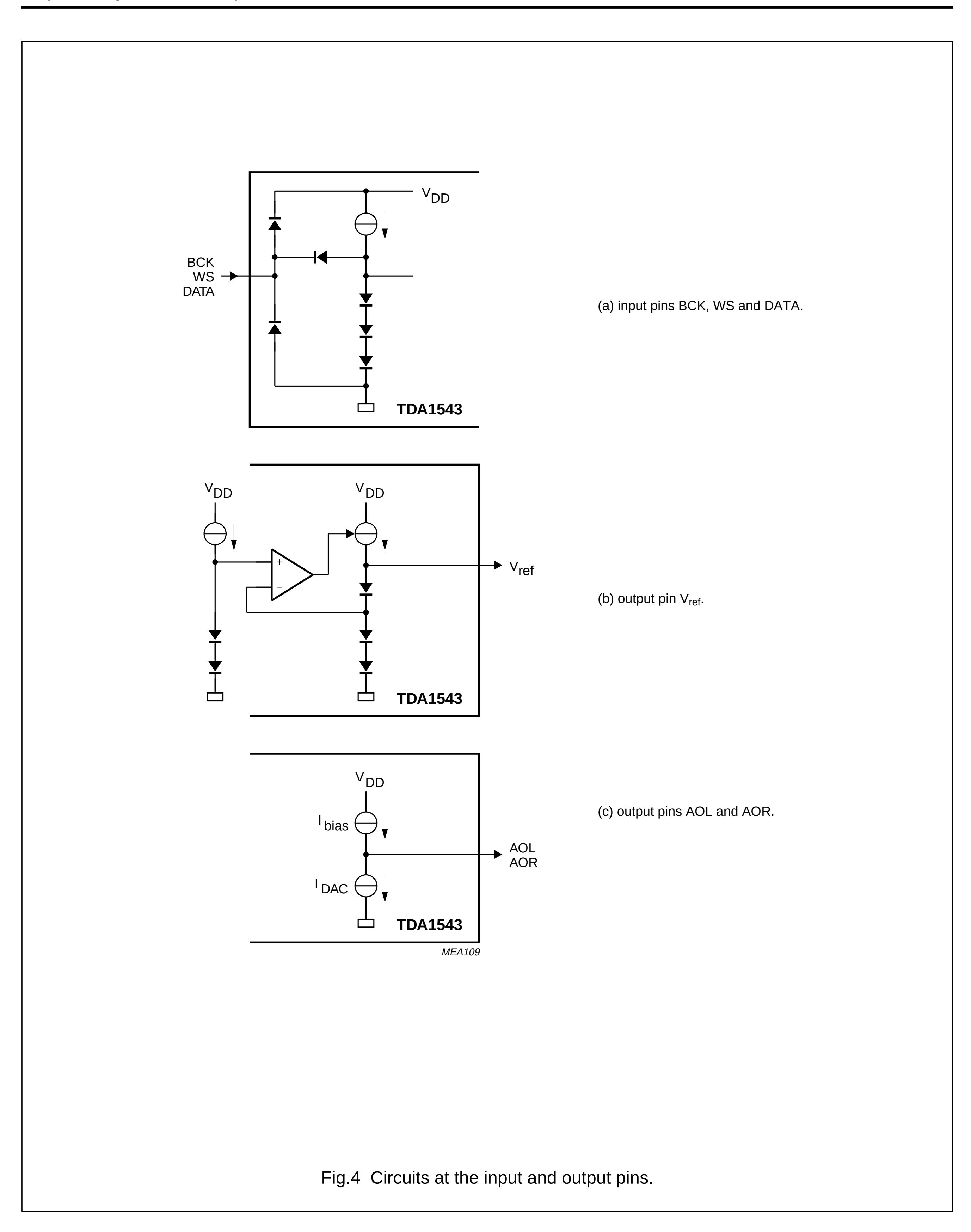


Fig.4 Circuits at the input and output pins.

FUNCTIONAL DESCRIPTION

The TDA1543 accepts input serial data formats in two's complement with any bit length. Left and right data words are time multiplexed. The most significant bit (bit 1) must always be first. The format of data input is shown in Fig.5 and Fig.6.

This flexible input data format (I^2S) allows easy interfacing with signal processing chips such as interpolation filters, error correction circuits and audio signal processor circuits (ASP).

The high maximum input bit-rate and fast settling current facilitates application in 4 × oversampling systems. An adjustable current is added to the output currents to bias output operational amplifiers (OP1; OP2) for maximum dynamic range (see Fig.1).

With a LOW level on the word select (WS) input data is placed in the left input register and with a HIGH level on the WS input data is placed in the right input register. The data in the input registers is simultaneously latched in the output registers which control the bit switches.

The output current of the DAC is a sink current. The current I_{ref} at the V_{ref} output is adjusted by a resistor or a current source. The current I_{ref} is amplified with gain A_{Ibias} to the bias currents (I_{BL}; I_{BR}) which are added to the output currents.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltage range		0	9	V
T_{XTAL}	crystal temperature		–	+150	°C
T_{stg}	storage temperature range		–55	+150	°C
T_{amb}	operating ambient temperature range		–30	+85	°C
V_{es}	electrostatic handling*		–2000	+2000	V

THERMAL RESISTANCE

SYMBOL	PARAMETER	TYP.	UNIT
$R_{th\ j\text{-}a}$	from junction to ambient	100	K/W

* Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

CHARACTERISTICS

V_{DD} = 5 V; T_{amb} = + 25 °C; I_{ref} = 0 mA; measured in the circuit of Fig.1; unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DD}	supply voltage range		3.0	5.0	8.0	V
I_{DD}	supply current	note 1	–	50	60	mA
RR	ripple rejection	note 2	–	50	–	dB
Digital inputs						
	input current pins (1, 2 and 3)					
I_{IL}	digital inputs LOW	V_I = 0.8 V	–	–	–0.4	mA
I_{IH}	digital inputs HIGH	V_I = 2.0 V	–	–	20	µA
	input frequency/bit rate					
f_{BCK}	clock input pin 1		–	–	9.2	MHz
BR	bit rate data input pin 3		–	–	9.2	Mbits/s
f_{WS}	word select input pin 2		–	–	192	kHz
Analog outputs (AOL; AOR)						
Res	resolution		–	–	16	bits
	output voltage compliance					
$V_{OC(AC)}$	AC		–	±25	–	mV
$V_{OC(DC)}$	DC		1.8	–	V_{DD}–1.2	V
I_{FS}	full scale current		1.95	2.30	2.65	mA
T_{CFS}	full scale temperature coefficient		–	$\pm 500 \times 10^{-6}$	–	K^{-1}
I_{offset}	offset current	I_{ref} = 0 mA	–0.1	0.0	0.1	mA
I_{bias}	bias current (adjustable)		–0.6	–	5.0	mA
AI_{bias}	bias current gain		1.9	2.0	2.1	
Analog outputs (V_{ref})						
V_{ref}	reference voltage output		2.10	2.20	2.30	V
I_{ref}	reference current output		–0.3	–	2.5	mA
THD	total harmonic distortion	including noise at 0 dB;		–75	–70	dB
		note 3, Fig.7		0.018	0.032	%
THD	total harmonic distortion	including noise at –60 dB;	–	–30	–23	dB
		note 3, Fig.7	–	3.2	7.9	%
t_{cs}	settling time ±1 LSB		–	0.5	–	µs
α	channel separation		85	90	–	dB
$\lvert d_{IO} \rvert$	unbalance between outputs	note 4	–	< 0.2	0.3	dB
$\lvert t_d \rvert$	time delay between outputs		–	< 0.2	–	µs
S/N	signal-to-noise ratio	at bipolar zero; note 5	90	96	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Timing (Fig.5**)**						
t_r	rise time		–	–	32	ns
t_f	fall time		–	–	32	ns
t_{CY}	bit clock cycle time		108	–	–	ns
t_{HB}	bit clock HIGH time		22	–	–	ns
t_{LB}	bit clock LOW time		22	–	–	ns
$t_{SU;DAT}$	data set-up time		32	–	–	ns
$t_{HD;DAT}$	data hold time to bit clock	note 6	2	–	–	ns
$t_{HD;WS}$	word select hold time	note 6	2	–	–	ns
$t_{SU;WS}$	word select set-up time		32	–	–	ns

Notes to the characteristics

1. Measured at I_{AOL} = 0 mA and I_{AOR} = 0 mA (code 8000H) and I_{bias} = 0 mA.
2. V_{ripple} = 1% of supply voltage and f_{ripple} = 100 Hz.
3. Measured with 1 kHz sinewave generated at a sampling rate of 192 kHz.
4. Measured with 1 kHz full scale sinewave generated at a sampling rate of 192 kHz.
5. At code 0000H.
6. At this point $t_{HD;DAT}$ = 0 ns, this value has been fixed on 2 ns due to tolerances.

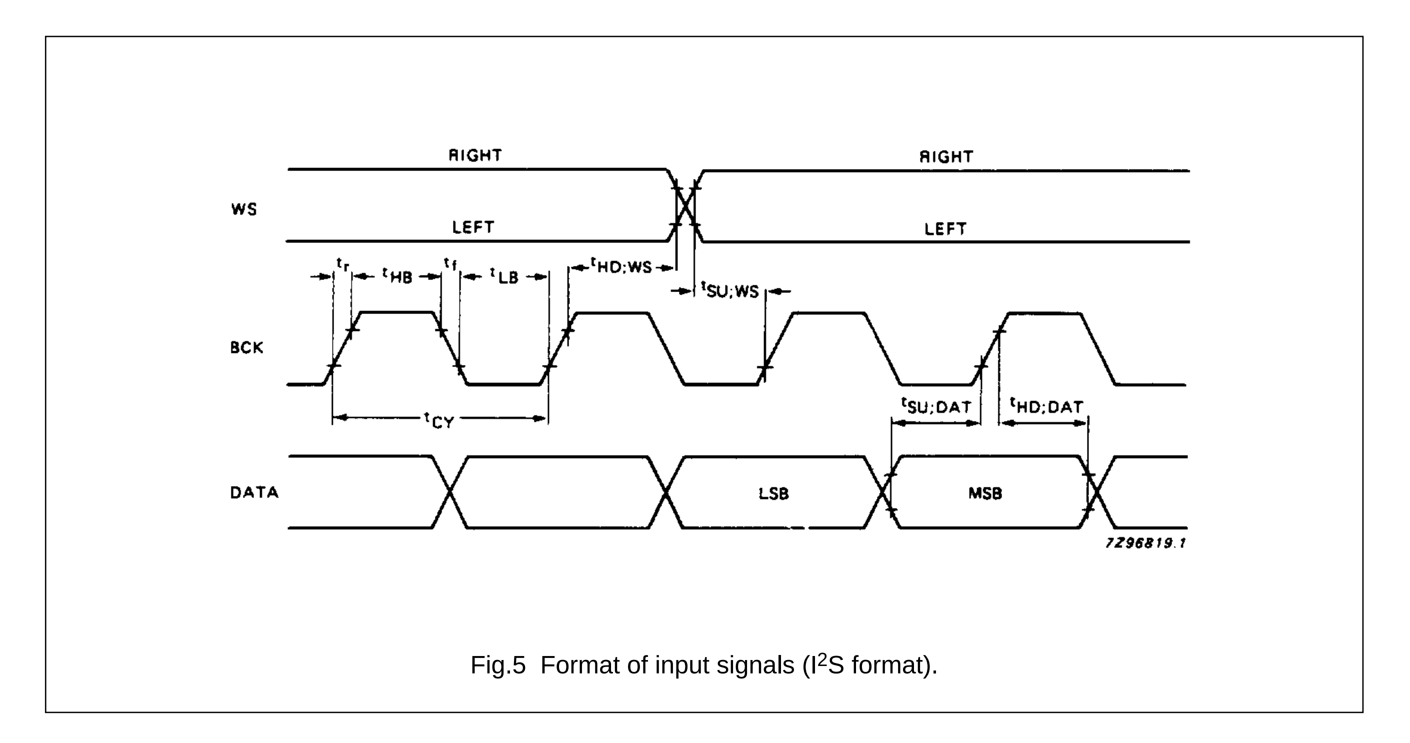


Fig.5 Format of input signals (I^2S format).

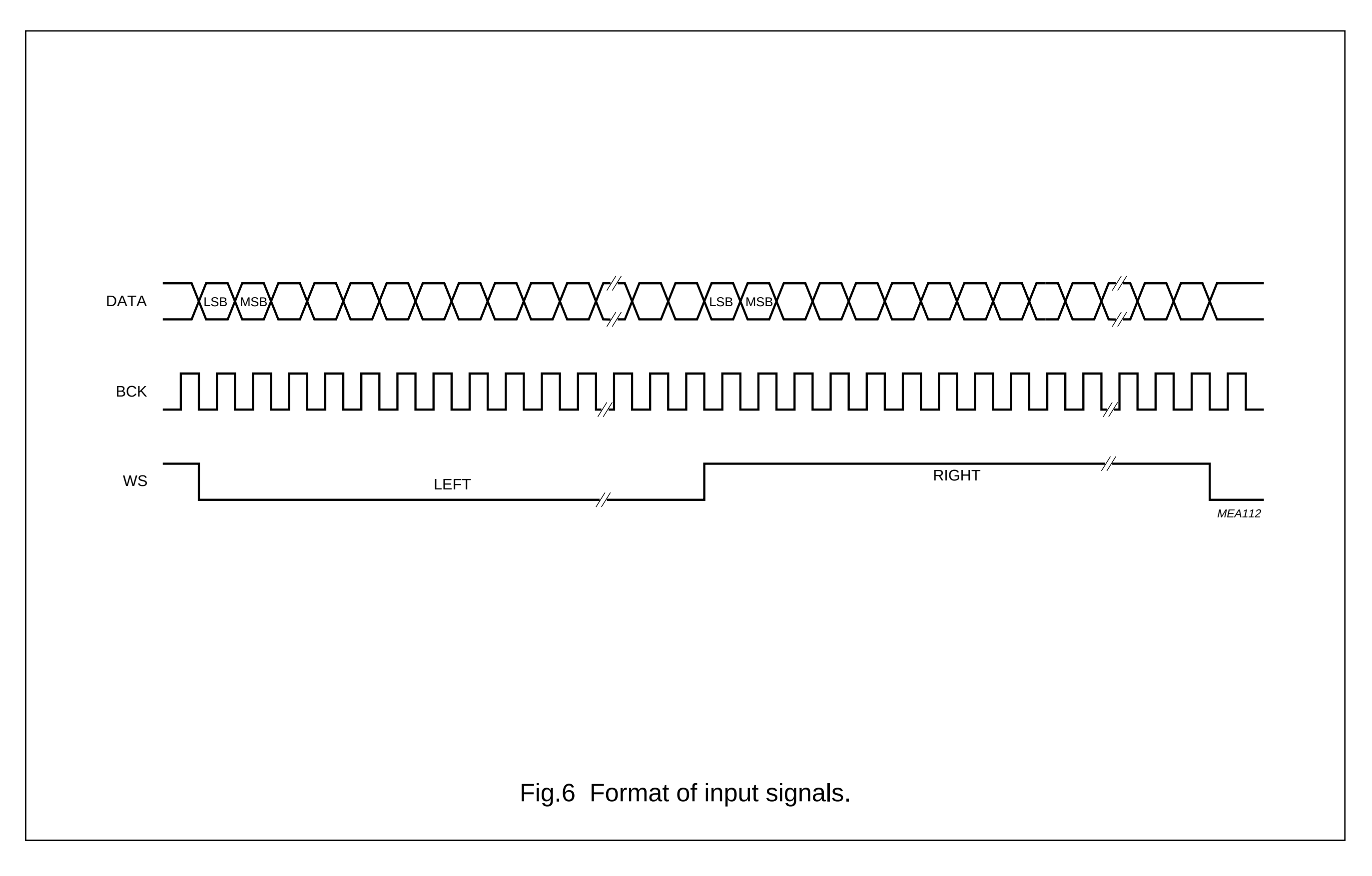
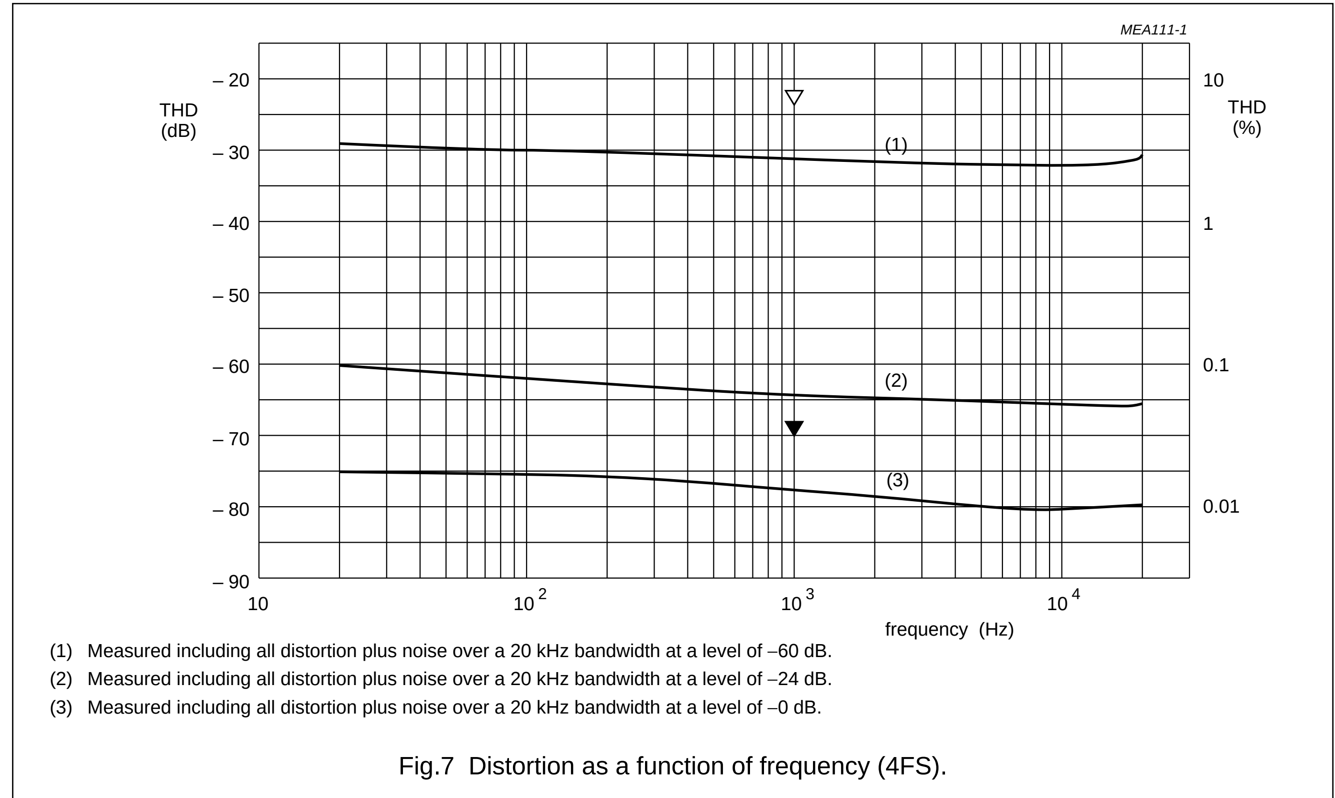


Fig.6 Format of input signals.



(1) Measured including all distortion plus noise over a 20 kHz bandwidth at a level of −60 dB.
(2) Measured including all distortion plus noise over a 20 kHz bandwidth at a level of −24 dB.
(3) Measured including all distortion plus noise over a 20 kHz bandwidth at a level of −0 dB.

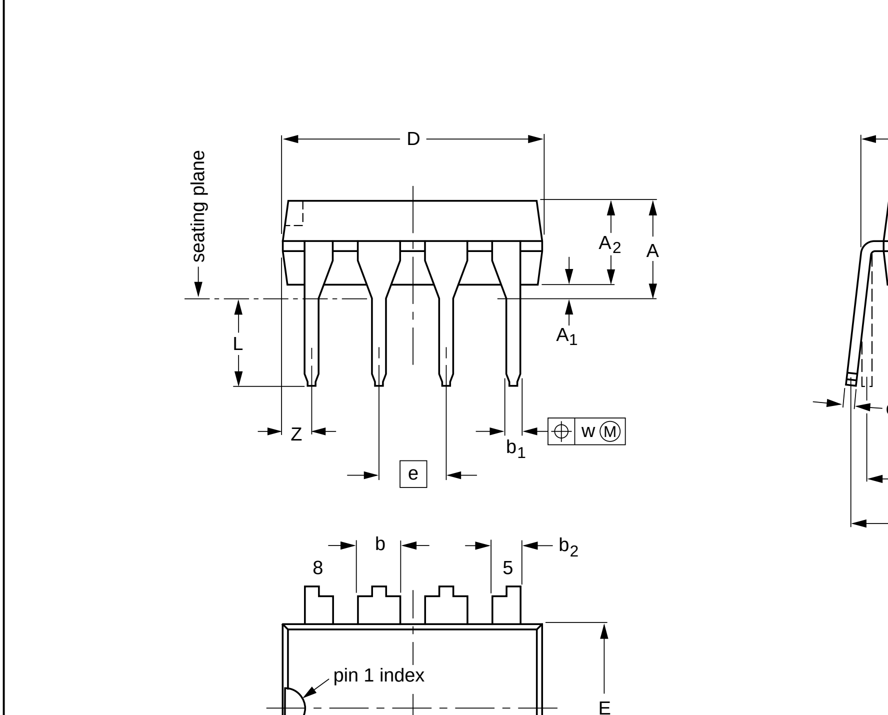
Fig.7 Distortion as a function of frequency (4FS).

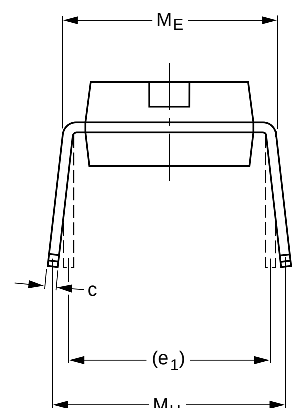
Notes to Fig.7

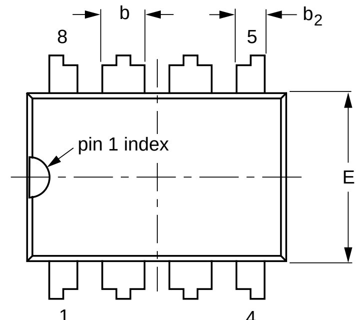
- The sample frequency 4FS: 176.4 kHz.
- The supply voltage at the measurement = + 5 V (DC).
- Ref: 0 dB is the output level of a full scale digital sine wave stimulus.
- The graphs are constructed from average values of a small amount of engineering samples therefore no guarantee for typical values is implied.
- The arrows indicate the specification limits for 0 dB and –60 dB level signals.

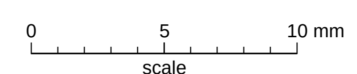
PACKAGE OUTLINES

DIP8: plastic dual in-line package; 8 leads (300 mil) **SOT97-1**









DIMENSIONS (inch dimensions are derived from the original mm dimensions)

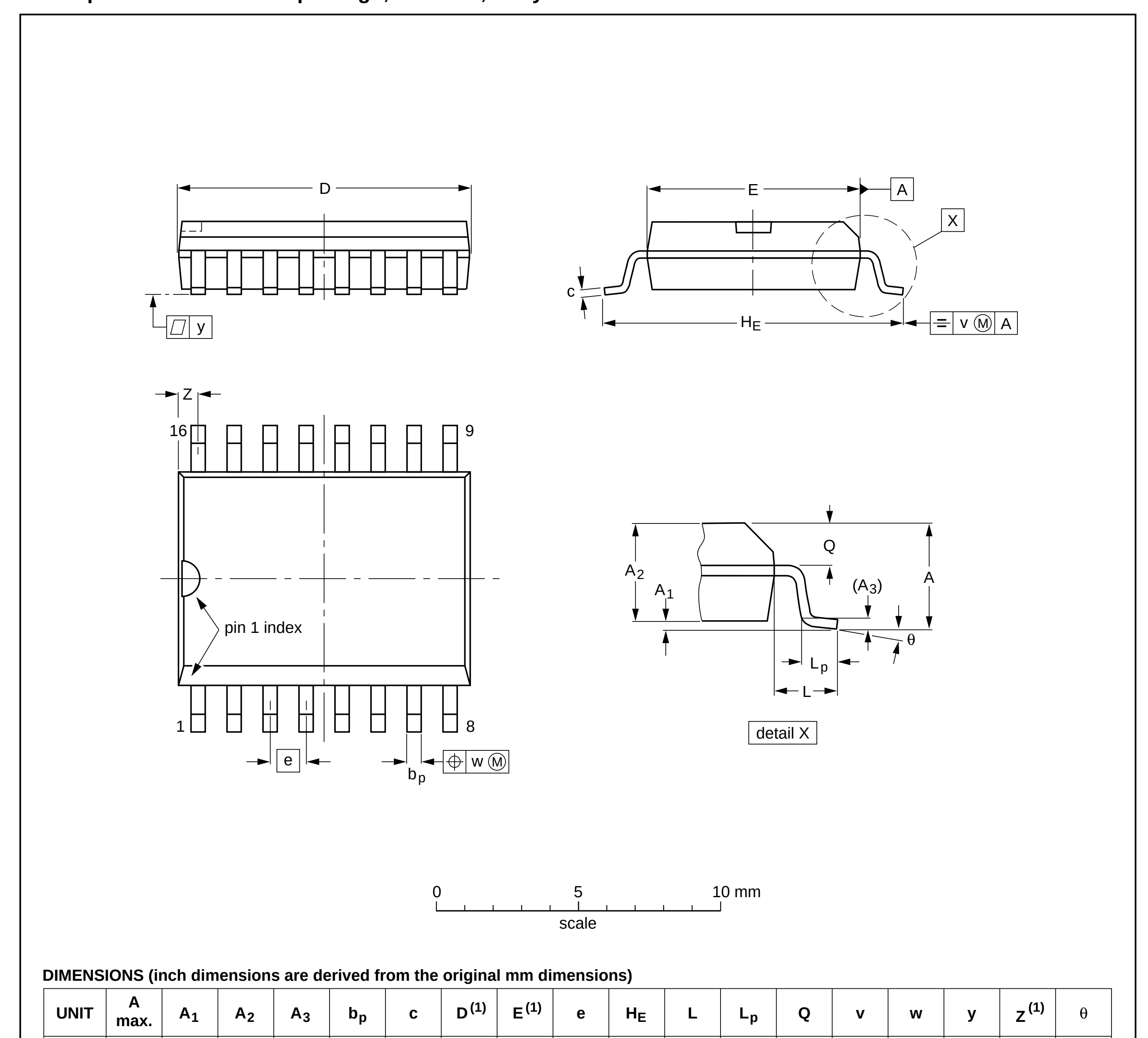
UNIT	A max.	A_1 min.	A_2 max.	b	b_1	b_2	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.2	0.51	3.2	1.73 1.14	0.53 0.38	1.07 0.89	0.36 0.23	9.8 9.2	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	1.15
inches	0.17	0.020	0.13	0.068 0.045	0.021 0.015	0.042 0.035	0.014 0.009	0.39 0.36	0.26 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.045

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT97-1	050G01	MO-001AN				~~92-11-17~~ 95-02-04

SO16: plastic small outline package; 16 leads; body width 7.5 mm **SOT162-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	10.5 10.1	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.41 0.40	0.30 0.29	0.050	0.42 0.39	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT162-1	075E03	MS-013AA				~~92-11-17~~ 95-01-24

SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

Soldering by dipping or by wave

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg\ max}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

Repairing soldered joints

Apply a low voltage soldering iron (less than 24 V) to the lead(s) of the package, below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.